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Nonlithographic Fabrication of Crystalline Silicon Nanodots on Graphene

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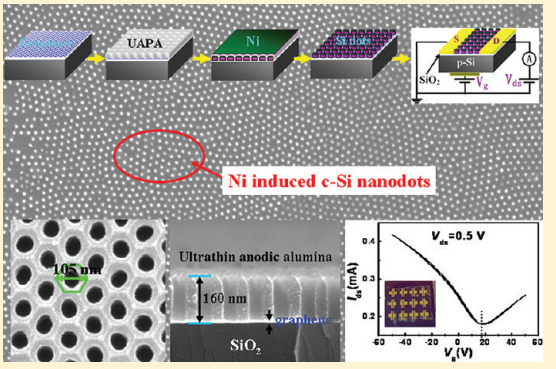
Supporting Information

ABSTRACT: We report a nonlithographic fabrication method to grow uniform and large-scale crystalline silicon (Si) nanodot (c-SiNDs) arrays on single-layer graphene by an ultrathin anodic porous alumina template and Ni-induced Si crystallization technique. The lateral height of the template can be as thin as 160 nm and the crystallization of Si can be achieved at a low temperature of 400 °C. The effects of c-SiNDs on graphene were studied by Raman spectroscopy. Furthermore, the c-SiNDs/graphene based field effect transistors were demonstrated.



1. INTRODUCTION

Graphene, a two-dimensional (2D) sp^2-bonded structure of carbon atoms arranged in a honeycomb lattice, has recently led to tremendous theoretical and research interests.[1−5] Its high intrinsic carrier mobility (~200 000 $cm^2V^{-1}s^{-1}$)[6] and near ballistic transport at room temperature[7] make it a promising candidate for future nanoelectronic applications, such as p-n junction diodes, high-speed field effect transistors (FET), and low-noise electronic and optical sensors.[8−10] Owing to the low density of states near the Dirac point and extremely large surface-to-volume ratio, single-layer graphene is very sensitive to modification by nanostructures.[11−15] Previous research has shown that graphene modified by semiconductor nanodots (SNDs) can provide a close-to-ideal transport pathway for charge carriers.[14,15] Some recent studies report on introducing random SNDs on reduced graphene oxides (RGOs).[14−18] However, the electrical characteristics of RGOs are undesirable because of the low charge carriers mobilities (<1 $cm^2V^{-1}s^{-1}$) and the hopping transport phenomenon between each adjacent RGO layers.[19] Therefore, SNDs directly grown on high quality single-layer graphene are necessary. Indeed, fabricating large-scale, high quality, and uniform SNDs on graphene is a very important step toward making graphene based micro- and nanoelectronic devices. By far, chemical vapor deposition (CVD) is the most successful and dominant method for fabricating large-scale and high crystalline graphene.[20] However, owing to the low binding energy for adsorbates on graphene,[21,22] our current effort is devoted to developing an innovative fabrication technique for preparing SNDs on pristine graphene.

Here, we report the use of ultrathin anodic porous alumina (UAPA) template and a nonlithographic approach to fabricate uniform SNDs on pristine single-layer graphene. Silicon is a standard semiconductor material for electronics nowadays. Si nanodots are very important for the development of new types of nanoelectronic devices.[23] So, the combination of graphene and Si nanodots can offer a unique possibility for fabricating high-performance nanodevices of the heterostructures and then to study their peculiar physical properties.

2. EXPERIMENTAL SECTION

2.1. Single-Layer Graphene Fabrication and Transfer. The commercial Cu foil (0.025-mm thick, Alfa Aesar, 99.8% in purity) was placed in a tube furnace and was heated up to 1000 °C. During the heating process, the Cu foil was kept under H_2 atmosphere with a gas flow rate of 10 sccm for 30 min. The chemical reaction occurred at the surface of heated Cu foil when CH_4 passed through. This process lasted 15 min. Then, the sample was cooled naturally

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in H_2 atmosphere. Concerning the transferring process, the protective layer polymethyl methacrylate (PMMA) was initially spin-coated onto one side of the as-prepared sample. The sacrificed Cu foil can be dissolved after being dipped into an iron chloride solution. Then, the graphene-coated PMMA has undergone a necessary cleaning process in order to get rid of the remaining metal flakes. The final step involves transferring graphene-coated PMMA onto SiO_2/Si substrate, and the PMMA can be easily removed by acetone.

2.2. Ultrathin Anodic Alumina Template Fabrication and Transfer. A high purity aluminum foil (99.999%) was used for making ultrathin anodic porous alumina (UAPA). The process requires a two-step electrochemical anodization in 0.3 M oxalic acid ($H_2C_2O_4$). Both aluminum foil and graphite plate were used as anode and cathode, respectively. During the first anodization, the DC voltage was set to be 40 V, the temperature of the solution is 5 °C and the time scale was 12 h. After the first anodization, a mixture of acids, 6.0 wt % H_3PO_4 and 1.8 wt % H_2CrO_4, was used to remove the anodic alumina oxide (AAO). The second anodization was conducted under the same experimental conditions as the first anodization. It needs 170 s to grow 160 nm UAPA. The 200 nm-thick PMMA was spin-coated onto one side of the UAPA template on Al substrate. The residual Al can be dissolved in a saturated $CuSO_4$ solution at room temperature in order to make a free-standing PMMA coated UAPA. The pore diameter can be further enlarged from 50 to 60 nm after dipping into 5 wt % H_3PO_4 at 30 °C for 45 min. Then, the free-standing PMMA coated UAPA was transferred onto graphene coated SiO_2/Si substrate.

2.3. Ni-Induced Crystalline Si Fabrication. The as-prepared UAPA coated graphene/SiO_2/Si was used as substrate. The deposition of Ni was carried out under the base pressure of 2×10^{-6} Torr at room temperature for 5 min by pulsed laser deposition (PLD). The 248 nm excimer laser with repetition rate of 4 Hz was used. Without breaking the vacuum, the Ni target was changed to an Si target. During the deposition of Si, the substrate temperature was set to 400 °C and the repetition rate of laser was 8 Hz for 10 min. In order to crystallize Si, subsequent annealing at the same temperature for 1 h was employed.

2.4. Characterization Methods. During the experiment, the graphene morphology was examined by transmission electron microscopy (TEM, JEOL-2010). Field emission scanning electron microscopy (FESEM, Sirion 200) was used to characterize the UAPA coverage, pore diameter, and the cross section. The depth profile of the as-fabricated nanodots was measured by atomic force microscopy (AFM, DI Nanocope 8). Raman spectroscopy (HORIBA) with excitation wavelength of 488 nm was used to study the monolayer graphene with and without nanodots. The electrodes for both drain and source were made by thermally evaporating 200 nm Au. The channel length and width were 100 μm and 2 mm respectively. Ag paste was used as the electrode for bottom gate. Prior to the electrical measurement in a glovebox filled with N_2, post annealing at 200 °C for 24 h was used to improve the contact between Au and the samples, and get rid of adsorbed oxygen and moisture. Some basic FET parameters, such as V_{ds}, I_{ds}, and V_g, were measured by semiconductor analyzer (Agilent 4156C).

3. RESULTS AND DISCUSSION

3.1. Nanofabrication Process of c-Si Nanodots on Graphene. In our scheme, the UAPA template with lateral thicknesses ranging from 80 nm to over 1 μm was obtained.[24] As shown in Figure 1a, a high purity Al foil is dealt with a two-step electrochemical anodization.[25] The schematic picture of the as-prepared UAPA is displayed in Figure 1b,c. The transferring process of the UAPA involves PMMA coating, residual polycrystalline Al (poly-Al) etching and pore widening. Prior to UAPA transfer and SNDs growth, a single-layer graphene was transferred onto SiO_2/Si substrate (Figure 1d,e). Then, the UAPA layer coated with PMMA, which is shown in Figure 1c, is transferred on top of the graphene/SiO_2 (0.3 μm)/Si (500 μm) (Figure 1f). The PMMA is dissolved in acetone (Figure 1g). Technically speaking, to fabricate large-scale crystalline Si nanodots (c-SiNDs) at low temperature (<500 °C) is highly desirable. If the temperature higher than 500 °C, for example close to the crystallization temperature of

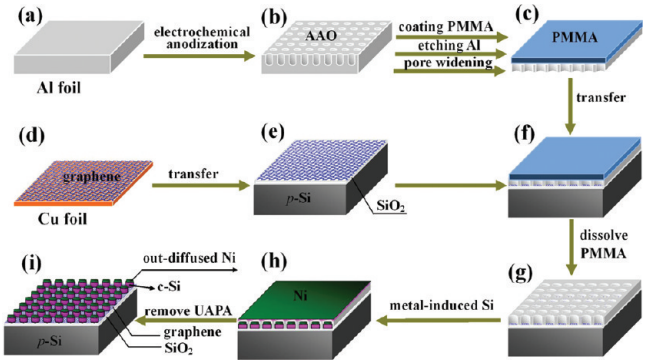

Figure 1. Schematic diagram of fabrication process for Ni-induced Si nanodots arrays on graphene: (a) Al foil; (b) Ultrathin anodic porous alumina (UAPA) fabricated by a two-step electrochemical anodization; (c) Transferring process includes PMMA coating, residual Al removing and pore widening; (d) Single-layer graphene prepared by CVD technique; (e) Transferring graphene onto SiO_2/Si substrate; (f) Transferring UAPA onto the graphene/SiO_2/Si; (g) Dissolving PMMA; (h) Ni-induced Si crystallization at 400 °C; and (i) Ni-induced c-Si nanodots formation.

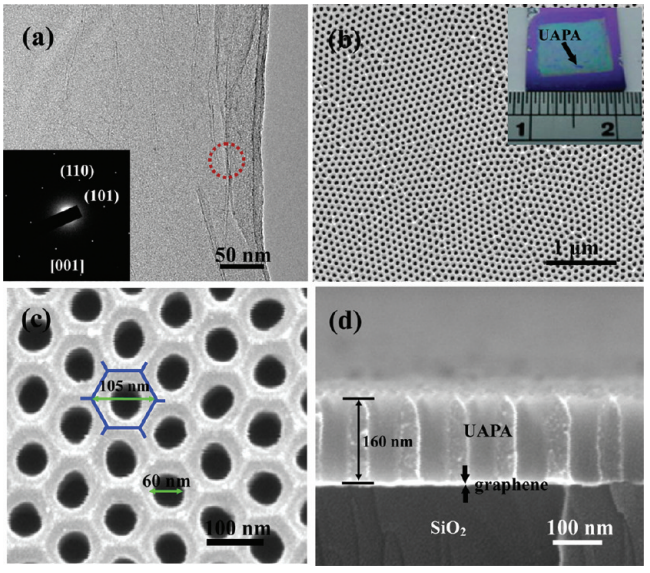

Figure 2. (a) TEM image of the single-layer graphene, inset shows corresponding electron diffraction pattern. (b) Top-view of SEM image of an UAPA template. Inset shows the image of the UAPA template on graphene/SiO_2/Si. (c) High resolution FESEM image of the UAPA. (d) Cross-sectional SEM image of the template.

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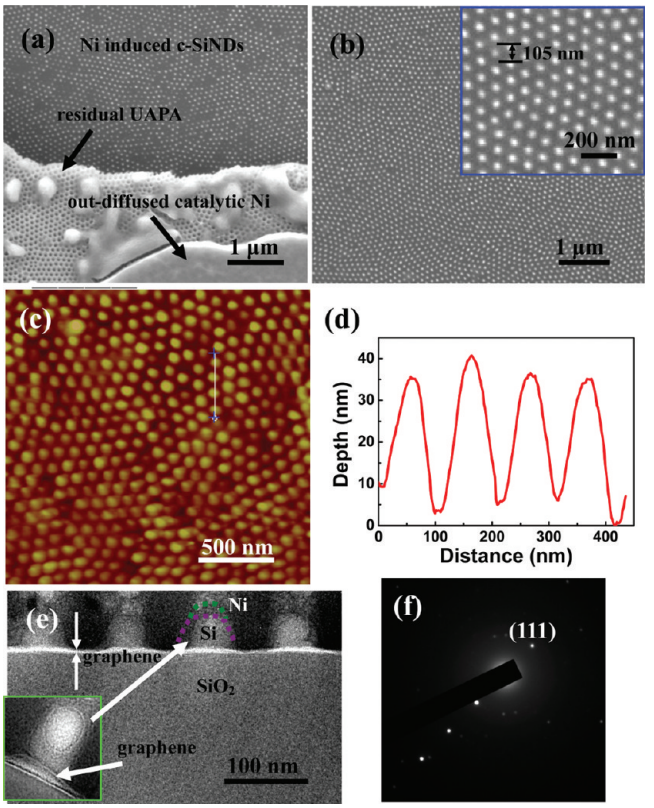

Figure 3. (a) Top-view FESEM image of the Ni-induced c-SiNDs on graphene with remaining UAPA template. (b) The well-ordered nanodot arrays on graphene after lift-off. (c) AFM image of the nanodots on single-layer graphene. (d) The corresponding depth profile of the nanodots on graphene. (e) Cross-sectional TEM image of the nanodots on graphene/SiO_2/Si. (f) The corresponding electron diffraction pattern of the Si nanodot.

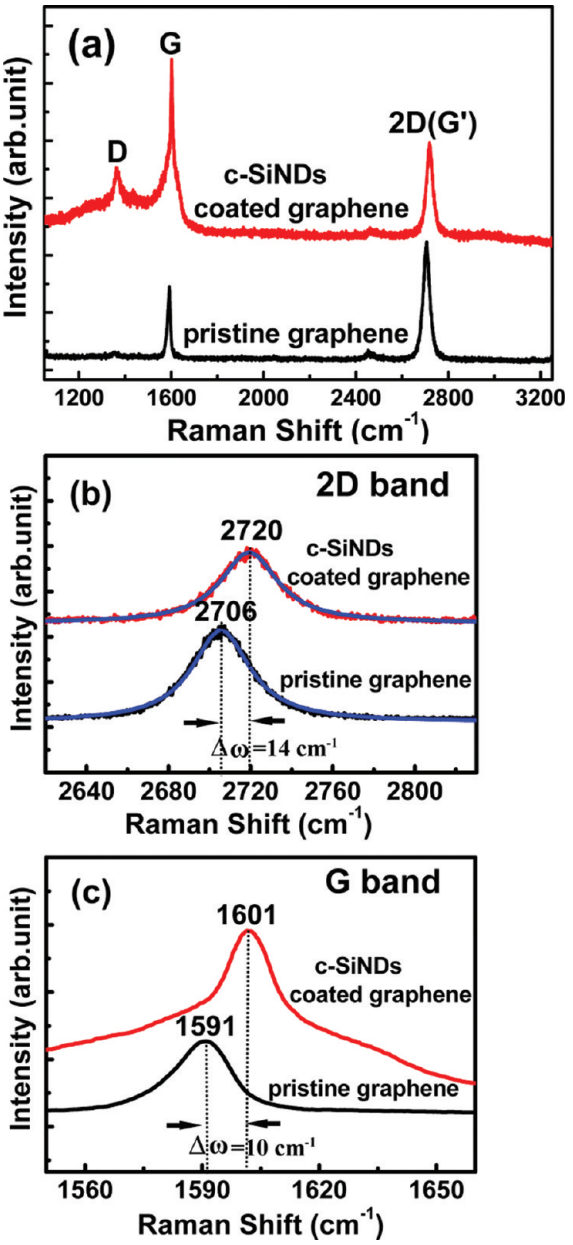

Figure 4. (a) Raman spectra of the single-layer graphene with (red) and without (black) c-SiNDs. (b) The Raman spectra of the 2D bands with Lorentzian fitting. (c) The Raman spectra of the G bands.

Si (>1000 °C),[26] then it will destroy the UAPA tempate. Here, we employed Ni-induced crystallization (NIC) method to fabricate c-SiNDs at 400 °C.[27] The catalytic Ni tends to form solid solution with Si at this temperature. The inter diffusion between Si and Ni leads to the nucleation and crystallization of Si inside each UAPA pore. Owing to the difference of concentration gradient in Si and Ni, the final step of the NIC is a completely interchange between Ni and Si (Figure 1h). Finally, a uniform c-SiND array on graphene can be obtained after removing the UAPA template. The corresponding schematic picture is shown in Figure 1i.

3.2. Structural and Morphology Characterization of c-Si Nanodots on Graphene. Figure 2a shows a TEM image of the pristine single-layer graphene. The red dotted circle indicates the presence of graphene ripples which is a typical characteristic of a single-layer graphene.[28] The selected area diffraction pattern (SADP) shown in the inset displays the hexagonal symmetry of the diffracted spots. Two of them have been clearly indexed with (110) and (101). The zone axis being [001] is perpendicular to all the electron diffracted spots. The inset of Figure 2b illustrates the photographic image of the UAPA template transferred on top of 1 cm^2 single-layer graphene/SiO_2/Si. Figure 2b shows a FESEM image of the UAPA template. Excellent self-ordering of the hexagonally close-packed alumina cells in each cell is observed. High magnification FESEM image in Figure 2c shows that the UAPA possesses a close-packed hexagonal array. For each cell, the cell size and the pore diameter are 105 and 60 nm, respectively. The cross-sectional FESEM image revealed in Figure 2d shows the straight parallel through-hole UAPA arrays with the lateral height of 160 nm. The interactive force between the UAPA and the graphene is by van der Waals' force.[29]

After partially removing the UAPA template, a number of Ni-induced c-SiNDs on graphene is exposed. In addition to this, the residual template together with out-diffused Ni layer can also be observed as shown in Figure 3a. Further evaluation of the area coverage of Ni-induced c-SiNDs can be observed from Figure 3b. According to the inset of Figure 3b, the average nanodot density based on the SEM images was calculated to be around 1.2×10^{10} /cm^2. The diameter of the nanodots is 60 nm, and the spacing between each pair of the nanodots is 105 nm. The result

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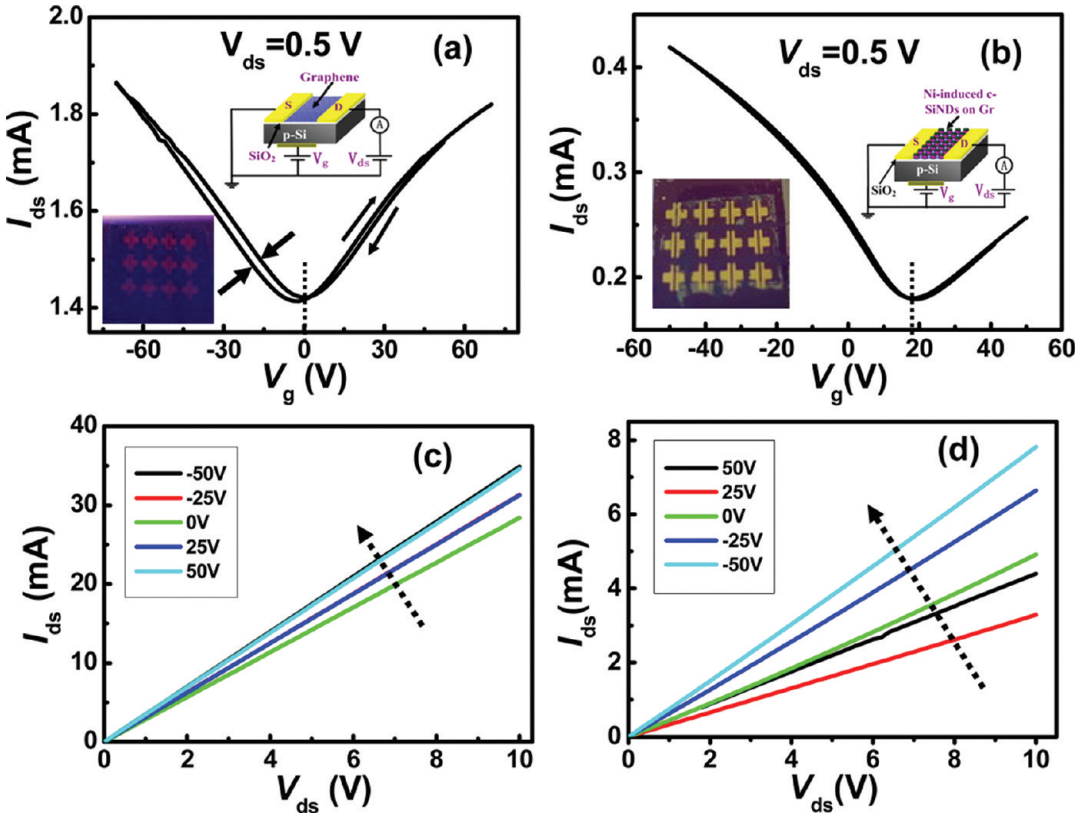

Figure 5. (a) I_{ds}-V_g transfer characteristics of a pristine single-layer graphene based FET device at V_{ds} = 0.5 V. The dotted lines indicate the Dirac point (the minimum conductance point). The V_g sweeping direction is indicated by the arrows. Inset shows an optical microscope image and schematic picture of the FET device layout. (b) I_{ds}-V_g transfer characteristics of Ni-induced c-SiNDs fabricated on graphene. Inset shows an optical microscope image and schematic picture of the FET device layout. (c) The corresponding I_{ds}-V_{ds} output characteristics of the graphene based FET tested at five different gate voltages (V_g = −50, −25, 0.0, 25, and 50 V). (d) The corresponding I_{ds}-V_{ds} output characteristics of c-SiNDs and graphene based FET tested at five different gate voltages (V_g = −50, −25, 0.0, 25, and 50 V).

is consistent with the previous observed interpore distance. The same sample was examined by AFM and the corresponding AFM image with 2 × 2 μm in area is shown in Figure 3c. Four nanodots in the AFM image were randomly chosen for depth profile measurement. Figure 3d indicates the lateral height of the as-prepared Ni-induced c-SiNDs is 35 ± 5 nm. Furthermore, as we can see from the TEM image in Figure 3e, four c-SiNDs are well aligned in a horizontal plane. The lateral height for each c-SiND is 35 nm which is consistent with the result of AFM depth profile measurement. The SADP (Figure 3f) captured for an individual NIC SiND indicates single crystalline quality.

Raman spectroscopy plays an important role in studying and characterizing graphitic materials, especially when considering heterostructures. Graphene, in this regard, can be identified in terms of number and orientation of layers by means of inelastic light scattering. Furthermore, it also performs as a probe for heterojunction induced strain effect. A common feature of pristine graphene is shown in Figure 4a. The graphitic (G) band which appears at 1591 cm^{-1} is due to C−C sp^2 bond. The G band corresponds to the E_{2g} phonon at the Brillouin zone center.[30] It represents the crystallinity of graphene. The band located at 2706 cm^{-1} is caused by double resonance process activated second-order Raman scattering near the boundary of the Brillouin zone of graphene.[31] It is usually denoted as Ǵ or 2D band. Moreover, it is recognized as a fingerprint for single-, bi-, and few-layer graphene.[32] For single-layer graphene, the 2D band shows a highly symmetric single peak. But for bilayer graphene, it tends to split into four components which correlated with four virtual transitions. In spite of this, the intensity ratio of I_{2D}/I_G is an alternative indicator to judge the number of graphene layers involved. For our CVD growth pristine graphene, the intensity ratio of I_{2D}/I_G is close to 0.5. This implies our graphene is single-layer.[20,33] Owing to the excellent crystalline quality, our graphene shows the absence of defective (D) band at 1364 cm^{-1}. Such a band is due to the breathing modes of sp^2 atoms and requires a defect for its activation.[30] By comparing the pure graphene sample, the Ni-induced c-SiNDs coated graphene exhibits an increased intensity ratio of I_{2D}/I_G up to 1.7 and a noticeable D band. According to Figure 4b, the 2D bands of the pristine graphene and the one with nanodots are well fitted by highly symmetric Lorentzian curves. Besides, there is no splitting of the 2D band, indicating that the only double resonance (DR) process for such decorated single-layer graphene.[34] Therefore, although the intensity ratio of I_{2D}/I_G is changed after the fabrication of nanodots, our experimental result reveals that it has no effect on the number of graphene layers. Moreover, the rise of D band is observed at 1364 cm^{-1}. We attribute the D band to ion implantation during PLD fabrication process because it is known that laser ablation is a process of producing high energetic species such as ions, atoms and molecules. In Figure 4b, a significant blue-shift of the 2D band by 14 cm^{-1} can be observed. We considered two primary reasons; one is thermal effect and the other is Ni-induced c-SiNDs. Nevertheless, we

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have found that the samples with the structure of single-layer graphene/SiO_2/Si, annealed at 400 °C in high vacuum (2×10^{-6} Torr) for 1 h yield the same Raman result as the one of pristine graphene without thermal treatment (Supporting Information, Figure S1). Therefore, we believe that the nanodots cause the blue-shift of the 2D band. In Figure 4c, the blue-shift of the G band by 10 cm^{-1} can also be observed for the sample with nanodots. Both blue-shifts are likely due to significant strain[35] and doping effect[21] of c-SiNDs in the graphene surface.

3.3. Field Effect Transistor Characterization of c-Si nanodots on Graphene. Figure 5a shows the I_{ds}-V_g transfer characteristic of the pristine graphene field effect transistor (FET) device. The V_{ds} was set to be 0.5 V. The I_{ds}-V_g curve consists of both hole branch (negative) and electron branch (positive). The curve exhibits a symmetric ambipolar transfer characteristic. In this case, the gate voltage (V_g) at the lowest point of the I_{ds}-V_g curve is known as the Dirac point or neutrality point (V_{dirac}). A slight mismatch of the hysteresis can be observed when the forward and the reverse V_g bias voltages are applied. This mismatch is primarily due to charge trapping effect in graphene.[36] During the CVD growth, the morphology or the grain size of graphene replicates that the Cu foil substrate. Charge accumulation at the grain boundaries can lead to charge scattering. Thus, charge trapping effect mainly comes from two mechanisms: one is material itself (single or polycrystalline materials) and the other is due to the fabrication technique. In our experiment, we found that the charge trapping effect can be greatly reduced when the Ni-induced c-SiNDs was introduced into graphene based FET device. The I_{ds}-V_g curve of the FET with Si nanodots is shown in Figure 5b. This also gives an asymmetric ambipolar transfer characteristic. However, the entire curve shifts to positive. As a consequence, the corresponding V_{dirac} is 18 V. Similar phenomenon was observed when potassium (K) doped into graphene.[37] Moreover, the major part of this I_{ds}-V_g curve is attributed to the hole branch, which indicates the injected charge carrier from nanodots to graphene is hole. This charge-transfer process lowers the Fermi level of the graphene, which results in p-type doping. On the basis of this I_{ds}-V_g curve, the excess hole concentration can be calculated as follows:[38]

$$n_{ex\text{-}h} = \frac{\varepsilon_0 \varepsilon_r}{e d_{OX}} \Delta V\mathrm{dirac} \quad (1)$$

where, ε_0 is the permittivity of vacuum, ε_r is the relative permittivity of SiO_2 (3.9), e is the electronic charge (1.602×10^{-19} C) and d_{ox} is the thickness of SiO_2 (300 nm). Thus, the calculated excess hole concentration, $n_{ex\text{-}h}$, is 1.280×10^{12} cm^{-2}. Besides, field effect mobility ($\mu_{e,h}$) can be calculated as follows:[39]

$$\mu_{e,h} = \frac{L}{W C_{ox} V_{ds}} \frac{\Delta I_{ds}}{\Delta V_g} \quad (2)$$

where L and W are the length and the width of the FET channel, respectively. C_{ox} is the gate oxide capacitance and can be expressed as $\varepsilon_{ox}\varepsilon_o/d_{ox}$. $\Delta I_{ds}/\Delta V_g$ is the transconductance in the linear regime of the I_{ds}-V_g curve. For the pristine graphene-based FET, the electron and hole mobilities are 65 $cm^2V^{-1}s^{-1}$ and 62 $cm^2V^{-1}s^{-1}$, respectively. The relatively low charge mobilities in our experiment are ascribed to long channel length (100 μm) which definitely increases the diffusion length for charge carriers. Some calculations were carried out for the sample with Ni-induced c-SiNDs, the electron and hole mobilities are 25 $cm^2V^{-1}s^{-1}$ and 43 $cm^2V^{-1}s^{-1}$, respectively. By comparison, the decrease in charge carriers mobilities are due to the introduction of some scattering centers within graphene. In addition, for the sample with nanodots, the difference between hole and electron mobilities is relatively large. This also verifies the fact that the majority charge carriers in our graphene are holes. Therefore, the Fermi energy level of the graphene has been reduced. Regarding the on/off current ratios for both samples (Figure 5a,b), the on/off ratio is increased from 1.2 to 2.3 at $V_g = -50$ V when nanodots are taken into account. Figure 5c,d, which corresponds to both samples in Figure 5a,b respectively, show the I_{ds}-V_{ds} output characteristics at five different V_g (−50 V, −25 V, 0.0 V, 25 and 50 V). Apparently, the sample with nanodot arrays has more degree of freedom on tuning I_{ds}-V_{ds} output characteristic.

4. CONCLUSIONS

We have demonstrated a nonlithographic method for c-SiNDs growth on graphene. The c-SiNDs were fabricated based on ultrathin anodic porous alumina template and Ni-induced crystallization. The spatial arrangement of c-SiNDs is well-defined by the transferable UAPA template. The interaction of c-SiNDs and graphene was investigated by Raman spectroscopy. In comparison with pure single-layer graphene, the blue shifts of both G and 2D bands in the c-SiNDs coated graphene are due to strain and doping effect. Field effect transistor measurements showed that the nanodots lead to the positive shift of V_{dirac} up to 18 V. In addition, due to the effect of nanodots, the on/off current ratio can be improved from 1.2 to 2.3. Therefore, our results indicate that this nanofabrication method has great potential for achieving functional optoelectronic devices such as photovoltaic and photodetectors.

■ ASSOCIATED CONTENT

Supporting Information. Figures showing the Raman spectra of the graphene before and after annealing and I_{ds}-V_g characteristics of the graphene and graphene decorated with Si nanodots. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

§These authors contributed equally to this work.

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